WHAT IS CLAIMED IS:

1   1.   A limited switch dynamic logic circuit comprising:

2   a dynamic node;

3   precharge circuitry coupled to said dynamic for precharging the dynamic node

4   to a logic one during a precharge cycle of a clock signal;

5   a logic tree coupled to said dynamic node for evaluating said dynamic node to

6   a logic one or a logic zero in response to combinations of logic states of plurality of

7   logic inputs coupled to said logic tree during an evaluation cycle of said clock signal;

8   static logic circuitry for latching a logic state of said dynamic node and

9   holding said logic state during said precharge cycle of said clock signal, wherein said

10   static logic circuitry generates said output and said complementary output; and

11   a keeper circuit having a keeper input coupled to said dynamic node, a keeper

12   output coupled to said dynamic node, a first supply terminal coupled to a first supply

13   signal, and a second supply terminal coupled to a second supply signal, wherein said

14   keeper output reinforces a first logic state of said dynamic node and does not

15   reinforce a second logic state of said dynamic node in response to logic states of said

16   first and second supply signals.

1   2.   The limited switch dynamic logic circuit of claim 1 further comprising a first

2   logic gate having a first mode input coupled to a first mode signal and a first mode

3   output coupled to said first supply terminal and generating said first supply signal,

4   wherein said first supply signal has said first logic state when said first mode signal

5   has said second logic state and said first supply signal has said second logic state

6   when said first mode signal has said first logic state.

1   3.   The limited switch dynamic logic circuit of claim 1 further comprising a

2   second logic gate having a second mode input coupled to a second mode signal, a

3   third mode input coupled to said first mode signal and a second mode output coupled

4   to said second supply terminal and generating said second supply signal, wherein said

5   second supply signal has said first logic state when said second mode signal has said

6   second logic state and said third mode output has said second logic state and said

7   second supply signal has said second logic state when either said first or second mode

8   signal has said first logic state.

1   4.   The limited switch dynamic logic circuit of claim 2, wherein said first logic

2   gate is an inverter logic gate.

1   5.   The limited switch dynamic logic circuit of claim 3, wherein said second logic

2   gate is a NOR logic gate.

1   6.   The limited switch dynamic logic circuit of claim 1, wherein said keeper

2   circuit comprises:

3   an inverter having an input coupled to said dynamic node, an inverter output,

4   a positive power supply input coupled to said first supply terminal, and a second

5   power supply input coupled to said second supply terminal; and

6   an electronic switch having an input coupled to said inverter output, a first

7   terminal coupled to said positive power supply voltage and a second terminal coupled

8   to said dynamic node, wherein said electronic switch couples said positive power

9   supply voltage to said dynamic node when said inverter output has said first logic

10   state and is OFF when said inverter output has said second logic state.

1   7.   The limited switch dynamic logic circuit of claim 6, wherein said inverter

2   comprises:

3   a first P channel field effect transistor (PFET) having a drain terminal coupled

4   to said positive power supply input, a source terminal, and a gate terminal coupled to

5   said dynamic node; and

6   a first N channel field effect transistor (NFET) having a drain terminal

7   coupled to said source terminal of said first PFET, a gate terminal coupled to said

8   dynamic node, and a source terminal coupled to said negative power supply input.

1   8.   The limited switch dynamic logic circuit of claim 7, wherein said electronic

2   switch comprises a second PFET having a gate terminal coupled to said inverter

3   output, a source terminal coupled to said positive power supply voltage and a drain

4   terminal coupled to said dynamic node.

1   9.   The limited switch dynamic logic circuit of claim 2, wherein said first mode

2   signal is a burn-in mode signal having said first logic state when a burn-in mode is

3   disabled and said second logic state when said burn-in mode is enabled.

1   10.   The limited switch dynamic logic circuit of claim 2, wherein said second

2   mode signal is a slow_ mode signal setting a fifty percent duty cycle clock mode,

3   wherein said slow_ mode signal enables a fifty percent duty cycle clock when said

4   slow_mode signal has said second logic state and enables a pulse clock when said

5   slow_mode signal has said first logic state.

1   11.   A logic device comprising:

2   a plurality of limited switch dynamic logic (LSDL) circuits wherein each of

3   said LSDL circuits has a dynamic node, precharge circuitry coupled to said dynamic

4   for precharging the dynamic node to a logic one during a precharge cycle of a clock

5   signal, a logic tree coupled to said dynamic node for evaluating said dynamic node to

6   a logic one or a logic zero in response to combinations of logic states of plurality of

7   logic inputs coupled to said logic tree during an evaluation cycle of said clock signal,

8   static logic circuitry for latching a logic state of said dynamic node and holding said

9   logic state during said precharge cycle of said clock signal, wherein said static logic

10   circuitry generates said output and said complementary output, and a keeper circuit

11   having a keeper input coupled to said dynamic node, a keeper output coupled to said

12   dynamic node, a first supply terminal coupled to a first supply signal, and a second

13   supply terminal coupled to a second supply signal, wherein said keeper output

14   reinforces a first logic state of said dynamic node and does not reinforce a second

15   logic state of said dynamic node in response to logic states of said first and second

16   supply signals.

1   12.   The logic device of claim 11 further comprising a first logic gate having a first

2   mode input coupled to a first mode signal and a first mode output coupled to said first

3   supply terminal and generating said first supply signal, wherein said first supply

4   signal has said first logic state when said first mode signal has said second logic state

5   and said first supply signal has said second logic state when said first mode signal has

6   said first logic state.

1   13.   The logic device of claim 11 further comprising a second logic gate having a

2   second mode input coupled to a second mode signal, a third mode input coupled to

3   said first mode signal and a second mode output coupled to said second supply

4   terminal and generating said second supply signal, wherein said second supply signal

5   has said first logic state when said second mode signal has said second logic state and

6   said third mode output has said second logic state and said second supply signal has

7   said second logic state when either said first or second mode signal has said first logic

8   state.

1   14.   The logic device of claim 11, wherein said keeper circuit comprises:

2   an inverter having an input coupled to said dynamic node, an inverter output,

3   a positive power supply input coupled to said first supply terminal, and a second

4   power supply input coupled to said second supply terminal; and

5   an electronic switch having an input coupled to said inverter output, a first

6   terminal coupled to said positive power supply voltage and a second terminal coupled

7   to said dynamic node, wherein said electronic switch couples said positive power

8   supply voltage to said dynamic node when said inverter output has said first logic

9   state and is OFF when said inverter output has said second logic state.

1   15.   The logic device of claim 12, wherein said first mode signal is a burn-in mode

2   signal having said first logic state when a burn-in mode is disabled and said second

3   logic state when said burn-in mode is enabled.

1   16.   The logic device of claim 12, wherein said second mode signal is a slow_

2   mode signal setting a fifty percent duty cycle clock mode, wherein said slow_ mode

3   signal enables a fifty percent duty cycle clock when said slow_mode signal has said

4   second logic state and enables a pulse clock when said slow_mode signal has said

5   first logic state.

1   17.   A data processing system comprising:

2   a central processing unit (CPU); and

3   a memory operable for communicating instructions and operand data to said

4   CPU, wherein said CPU includes a logic system having a logic device, said logic

5   device including a plurality of limited switch dynamic logic (LSDL) circuits wherein

6   each of said LSDL circuits has a dynamic node, precharge circuitry coupled to said

7   dynamic for precharging the dynamic node to a logic one during a precharge cycle of

8   a clock signal, a logic tree coupled to said dynamic node for evaluating said dynamic

9   node to a logic one or a logic zero in response to combinations of logic states of

10   plurality of logic inputs coupled to said logic tree during an evaluation cycle of said

11   clock signal, static logic circuitry for latching a logic state of said dynamic node and

12   holding said logic state during said precharge cycle of said clock signal, wherein said

13   static logic circuitry generates said output and said complementary output, and a

14   keeper circuit having a keeper input coupled to said dynamic node, a keeper output

15   coupled to said dynamic node, a first supply terminal coupled to a first supply signal,

16   and a second supply terminal coupled to a second supply signal, wherein said keeper

17   output reinforces a first logic state of said dynamic node and does not reinforce a

18   second logic state of said dynamic node in response to logic states of said first and

19   second supply signals.

1   18.   The data processing system of claim 17 further comprising a first logic gate

2   having a first mode input coupled to a first mode signal and a first mode output

3   coupled to said first supply terminal, wherein said first mode output has said first

4   logic state when said first mode signal has said second logic state and said first mode

5   output has said second logic state when said first mode signal has said first logic state.

1   19.   The data processing system of claim 17 further comprising a second logic gate

2   having a second mode input coupled to a second mode signal, a third mode input

3   coupled to said first mode signal and a second mode output coupled to said second

4   supply terminal, wherein said second mode output has said first logic state when said

5   second mode signal has said second logic state and said third mode output has said

6   second logic state and said second mode output has said second logic state when

7   either said first or second mode signal has said first logic state.

1   20.   The data processing system of claim 17, wherein said keeper circuit

2   comprises:

3   an inverter having an input coupled to said dynamic node, an inverter output,

4   a positive power supply input coupled to said first supply terminal, and a second

5   power supply input coupled to said second supply terminal; and

6   an electronic switch having an input coupled to said inverter output, a first

7   terminal coupled to said positive power supply voltage and a second terminal coupled

8   to said dynamic node, wherein said electronic switch couples said positive power

9   supply voltage to said dynamic node when said inverter output has said first logic

10   state and is OFF when said inverter output has said second logic state.

1   21.   A limited switch dynamic logic circuit comprising:

2   a dynamic node;

3   precharge circuitry coupled to said dynamic for precharging the dynamic node

4   to a logic one during a precharge cycle of a clock signal;

5   a logic tree coupled to said dynamic node for evaluating said dynamic node to

6   a logic one or a logic zero in response to combinations of logic states of plurality of

7   logic inputs coupled to said logic tree during an evaluation cycle of said clock signal;

8   static logic circuitry for latching a logic state of said dynamic node and

9   holding said logic state during said precharge cycle of said clock signal, wherein said

10   static logic circuitry generates said output and said complementary output; and

11   a keeper circuit having a keeper input coupled to said dynamic node, a keeper

12   output coupled to said dynamic node, a first supply terminal coupled to a first supply

13   signal, and a second supply terminal coupled to a second supply signal, wherein said

14   keeper circuit is selectively enabled during a burn-in mode and a slow clock mode by

15   logic states of said first and second supply signals.